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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,471	02/26/2004	Youn-Cheul Kim	SEC.1083	9314
20987	7590	09/21/2006	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			FLOURNOY, HORACE L	
		ART UNIT	PAPER NUMBER	
			2189	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,471	KIM, YOUN-CHEUL	
	Examiner Horace L. Flournoy	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 23 June 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3,5,7-9,11,13 and 15 is/are rejected.
- 7) Claim(s) 4,6,10,12,14 and 16 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 7-9, 11, 13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Toda (U.S Patent No. 6,363,465 hereafter referred to as Toda).

With respect to **independent claims 1 and 15**,

"An input/output data pipeline circuit of a semiconductor memory device, [See FIGs. 2, 3] comprising: a control signal generating unit [See FIG. 2, element 23] adapted to receive a clock signal [See FIG. 2, "CLK"] and adapted to output a control signal, [See FIG. 2, "CLK3"] a first switching signal, [See FIG. 2, "CLK1"] and a second switching signal, [See FIG. 2, "CLK2"] according to a frequency of the clock signal; [Toda teaches the usage of a high-frequency and a low-frequency clock signal changing the output of the pipeline circuit. See column 1, line 63 - column 2, line 4] a first transmitting unit [See

FIGs. 2,3, element 18. See column 11, lines 49-52] adapted to receive data stored in a memory cell [See FIGs. 2,3 element 12: "Memory Cell Array"] and to transmit data to an input/output driver [See FIGs. 2,3 element 22: "Output Driver". The "output driver" is analogous to the input/output driver as interpreted by the examiner] in response to activation of the first switching signal and the second switching signal; [See column 10, lines 50-57. Toda teaches that the first and second switching signals can be activated or controlled by the control signal SLTC, which is used to select the latency of the device.] and a second transmitting unit [See FIGs. 2,3, element 21] adapted to transmit data to the input/output driver in response to activation of the control signal, [See FIGs. 2,3 element 22: "Output Driver". See FIG. 2, "CLK3" which is the control signal for the input/output driver.] wherein the first transmitting unit and the second transmitting unit are adapted to be alternatively activated." [The timing diagram of FIG. 15, e.g., shows the "CLK1" (control for the first transmitting unit) and "CLK2" (control for the second transmitting unit) are alternately activated.]

With respect to independent claims 7 and 15,

"A semiconductor memory device comprising: a memory cell core, which includes a plurality of memory cells; [Toda discloses in column 10, lines 58-61, "The memory cell array 12 contains memory cells arranged in a matrix form such that the memory cells in each row are connected to a word line WL and the memory cells in each column are connected to a bit line BL."] an input/output driver [See FIGs. 2,3 element 22: "Output Driver". The "output

"driver" is analogous to the input/output driver as interpreted by the examiner] adapted to receive first data from outside of the semiconductor memory device, [See column 10, lines 50-57. Toda teaches that the control signal SLTC transmits data from outside the semiconductor memory device and sends the data (control) to the output driver. See FIG. 2.] in synchronization with a first clock signal, and adapted to output second data stored in the memory cell core, in synchronization with a second clock signal; [See column 2, lines 45-55.] an input/output data pipeline circuit, which is connected to the memory cell core and the input/output driver, [See FIGs. 2,3] which is adapted to transmit the second data stored in the memory cell core to the input/output driver, [See in FIGs. 2,3 the connection between the Memory Cell Array and the Output Driver.] and which is adapted to transmit the first data received from outside of the semiconductor memory device to the memory cell core; and a control signal generating unit, [See FIG. 2, element 23] which is adapted to receive the first clock signal and the second clock signal, [See column 2, lines 45-55. Toda teaches an external and internal clock signal.] and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal, [Toda teaches the usage of a high-frequency and a low-frequency clock signal changing the output of the pipeline circuit. See column 1, line 63 - column 2, line 4] wherein the input/output data pipeline circuit includes a first transmitting unit, which is adapted to perform a transmission operation between the memory cell core and the input/output driver in response to activation of a first switching signal and a second switching signal, [See FIGs. 2,3, element 18. See column

11, lines 49-52] and a second transmitting unit which ~~which is adapted to~~ perform a transmission operation between the memory cell core and the input/output driver in response to activation of the control signal, [See FIGs. 2,3, element 21. See all associated text within specification.] and wherein the first transmitting unit and the second transmitting unit are ~~adapted~~-adapted to be alternatively activated." [The timing diagram of FIG. 15, e.g., shows the "CLK1" (control for the first transmitting unit) and "CLK2" (control for the second transmitting unit) are alternately activated.]

With respect to **claims 2, 9, and 15**,

"The input/output data pipeline circuit of claim 1, wherein the first transmitting unit [See FIGs. 2,3, element 18. See column 11, lines 49-52] comprises: a first switching circuit adapted to output data in response to activation of the first switching signal; [See FIG. 2, "CLK1"] a latching circuit ~~adapted~~ adapted to latch and output the output of the first switching circuit; [See FIG. 2, element 18: "Latch Circuit". As interpreted by the examiner, the latch circuit of Toda, handles both "switching" and "latching."] and a second switching circuit adapted to output the output of the latching circuit to the input/output driver [See FIG. 2, elements 21, 26, and 22.] in response to activation of the second switching signal." [See FIG. 2, "CLK2"]

With respect to **claim 3**,

"The input/output data pipeline circuit of claim 1, wherein the second transmitting unit comprises a third switching circuit, which is adapted to output data to the input/output driver in response to activation of the control signal." [This claim is taught by Toda, e.g. in column 16, lines 17-31.]

With respect to **claims 5 and 11**,

"The input/output data pipeline circuit of claim 4, wherein the first switching signal is activated prior to activation of the second switching signal." [The timing diagram of FIG. 15, e.g., shows the "CLK1" signal activated prior to "CLK2".]

With respect to **claim 8**,

"The semiconductor memory device of claim 7, wherein the control signal generating unit [See FIG. 2, element 23] which is adapted to detect a phase difference between the first clock signal and the second clock signal, and which is adapted to output the control signal with a logic state based on a detected result." [See column 26, lines 36-54.]

With respect to **claims 13 and 15**,

"The semiconductor memory device of claim 7, wherein the control signal generating unit is further adapted to receive information about operation modes of the semiconductor memory device, and the control signal corresponds to the first clock signal, the second clock signal, and information about operation modes

of the semiconductor memory device." [Toda discloses this limitation, e.g. in column 2 line 62 – column 3, line 5.]

Allowable Subject Matter

Claims 4, 6, 10, 12, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

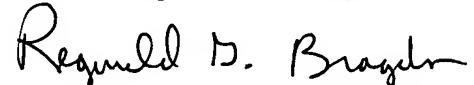
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy



Patent Examiner
Art unit: 2189

Reginald G. Bragdon



Supervisory Patent Examiner
Technology Center 2100